Application No. (if known): 10/757,241 Attorney Docket No.: 60568 (71987)

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One Month Request for Extension of Time Under 37 CFR 1.136(a) (2 pages)
Fee Transmittal (2 pages)
Request for Continued Examination Transmittal (1 page)
Copy of Amenment filed on November 3, 2005 (6 pages)
Return Receipt Postcard
Charge $910.00 to deposit account 04-1105

PTO/SB/17 (12-04v2)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 910.00

Complete if Known	
Application Number	10/757,241-Conf. #4373
Filing Date	January 14, 2004
First Named Inventor	Han-Ping Pu
Examiner Name	M. N. Tang
Art Unit	2829
Attorney Docket No.	60568 (71987)

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 04-1105 Deposit Account Name: Edwards Angell Palmer & Dodge LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - =	_____ x	_____ =	_____

Multiple Dependent Claims: Fee ($) _____ Fee Paid ($) _____

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - =	_____ x	_____ =	_____

3. APPLICATION SIZE FEE

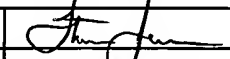
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ /50	_____ (round up to a whole number) x	_____ =	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1251 Extension for response within first month	120.00
1801 Request for continued examination (RCE) (see 37 ...	790.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent)	42,693	Telephone	(617) 439-4444
Name (Print/Type)	Steven M. Jensen			Date	December 5, 2005

Docket No. 60568 (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: H. Pu

U.S. SERIAL NO.: 10/757,241 GROUP: 2829

FILED: January 14, 2004 EXAMINER: M. Tang

FOR: WAFER TEST METHOD UTILIZING CONDUCTIVE INTERPOSER

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted by facsimile to the U.S. Patent & Trademark Office by facsimile number 571-273-8300 on November 3, 2005.

By: _____
Steven M. Jensen

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

AMENDMENT

Applicant is in receipt of the Office Action dated August 4, 2005 of the above-referenced application. Please amend the application as follows:

Amendments to the claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A wafer test method, comprising the steps of:

providing a wafer integrally formed of a plurality of chips, each of the chips having an active surface and an opposite inactive surface, with a plurality of bond pads formed on the active surface;

preparing a conductive interposer composed of a plurality of interposer units each corresponding to one of the chips, each of the interposer units having a first surface and an opposite second surface, wherein the first surface of each of the interposer units is formed with a solder mask having a plurality of openings and a plurality of test pads exposed via the openings of the solder mask, and the second surface of each of the interposer units is formed with a plurality of test bumps electrically connected to the test pads, the test bumps corresponding to the bond pads of the chips, and mounting the conductive interposer on the wafer such that the test bumps are in electrical contact with the bond pads to electrically connect the conductive interposer to the chips; and

using test probes to contact the test pads of the conductive interposer to perform tests for the chips of the wafer.

Claim 2 (canceled)

Claim 3 (original): The wafer test method of claim 1, wherein edges of the conductive interposer are supported by a frame that abuts against the wafer to position the conductive interposer on the wafer.

Claim 4 (original): The wafer test method of claim 1, wherein the conductive interposer comprises a core having the first surface and the second surface, a plurality of conductive traces formed on the first surface and the second surface of the core, and a plurality of conductive vias penetrating the core for electrically connecting the conductive traces on the first and second surfaces of the core.

Claim 5 (original): The wafer test method of claim 4, wherein the core is a thin film.

Claim 6 (original): The wafer test method of claim 4, wherein the core is a substrate made of an organic material.

Claim 7 (original): The wafer test method of claim 6, wherein the organic material is selected from the group consisting of epoxy resin, polyimide resin, BT (bismaleimide triazine) resin, and FR4 resin.

Claim 8 (original): The wafer test method of claim 4, wherein the conductive traces are made of copper.

Claim 9 (original): The wafer test method of claim 4, wherein the conductive vias are formed by plating copper in a plurality of through holes penetrating the core.

Claim 10 (currently amended): The wafer test method of claim 4, wherein ~~a~~ the solder mask is applied over the first surface of the core and formed with ~~a~~ the plurality of openings for exposing predetermined portions of the conductive traces, and the exposed portions serve as the test pads.

Claim 11 (original): The wafer test method of claim 10, wherein a solder mask is applied over the second surface of the core and formed with a plurality of openings for exposing predetermined portions of the conductive traces, allowing the test bumps to be bonded to the exposed portions.

Claim 12 (original): The wafer test method of claim 11, wherein the test bumps are electrically connected to the test pads by the corresponding conductive traces and conductive vias.

Claim 13 (original): The wafer test method of claim 11, wherein the test bumps are electrically connected and redistributed to the test pads by the corresponding conductive traces and conductive vias.

Claim 14 (original): The wafer test method of claim 1, wherein the test bumps are made of gold.

REMARKS

Claims 1 and 3-14 are pending in the application. Claim 1 has been amended by the present amendment to recite that each of the interposer units is formed with a solder mask having a plurality of openings and a plurality of test pads exposed via the openings of the solder mask. Claim 10 has been amended to properly agree with claim 1. The amendments are fully supported by the application as originally filed (see specification at page 7, fourth paragraph; FIG. 2C).

Applicant's claimed invention is directed to a wafer test method including a conductive interposer disposed between and electrically connected to a wafer and test probes, in order to prevent the test probes from directly contacting and damaging bond pads on the wafer during a test.

For example, as shown in FIG. 2C, a first surface of each interposer unit (of the conductive interposer) is formed with a solder mask 39 having a plurality of openings 390 and a plurality of test pads 33 exposed via the openings of the solder mask 39, such that the test probes contact the exposed test pads 33 to perform a test on the wafer (see specification at page 7, fourth paragraph).

Claims 1 and 3-14 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 5,559,446 to Sano. This rejection is respectfully traversed.

Sano does not teach or suggest a wafer test method in which a solder mask is formed on the first surface of a conductive interposer, and test pads are exposed via openings in the solder mask.

Referring to FIGS. 1 and 2 of Sano, a probe card 2 or card body 20 "is formed with connecting through holes 22 ... arranged at the outer circumferential portion thereof," so as to be in contact with pogo pins 51 (see column 4, lines 25-30).

As described in column 5, line 16 to column 6, line 3 of Sano, when performing a test, a heater 1 is turned on to heat the wafer W up to 80° to 150°C, and the wafer W and a thin substrate 4 expand at about the same rate, such that a dislocation rate of electrode pads on the wafer W is almost equivalent to that of the bumps 41 on the probe card 2 "to keep the reliable mutual positional relationship with respect to each other."

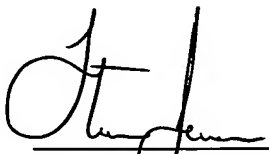
In other words, Sano addresses a problem in the prior art of positional dislocation between bumps and electrode pads in response to temperature change, e.g., due to a large difference in coefficient of thermal expansion (CTE) between a flexible thin film resin and a silicon wafer. In Sano, as the bumps 41 are dislocated when the thin substrate 4 expands, the connecting through holes 22 would not be formed at an area corresponding to the bumps 41.

On page 4, second paragraph of the Office Action of 08/04/2005, it was alleged that part of the wiring substrate 3 applied over the upper surface of the core 20 in Sano corresponds to Applicant's claimed "solder mask." However, in Sano, the upper surface of wiring substrate 3 is formed with a grounding layer 30 and connecting through holes 22, but **not** with a solder mask.

For at least the reasons discussed above, Sano does not anticipate or otherwise render obvious the Applicant's claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



Date: November 3, 2005

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